

WHAT IS CLAIMED IS:

1. A method for refreshing a memory device, comprising:
 - providing a memory cell having first and second memory locations;
 - generating a first updated latch value;
 - writing the first updated latch value to the first memory location;
 - generating a second updated latch value; and
 - writing the second updated latch value to the second memory location.
2. The method of claim 1, wherein generating the first updated latch value includes performing a logic operation on a value of the first memory location and a first data value.
3. The method of claim 2, wherein generating the second updated latch value includes performing a logic operation on a value of the second memory location and a second data value.
4. The method of claim 2, wherein performing the logic operation includes ORing the value of the first memory location and the first data value.
5. The method of claim 4, wherein generating the second updated latch value includes performing a logic operation on a value of the second memory location and a second data value.
6. The method of claim 5, wherein performing the logic operation includes ORing the value of the second memory location and the second data value.
7. The method of claim 1, wherein writing the first updated latch value to the first memory location includes latching the first updated latch value in response to at least one control signal.
8. The method of claim 7, wherein the at least one control signal comprises a first control signal indicative of a value of a first data value and a second control signal indicative of a status of a read operation.

9. The method of claim 8, wherein writing the second updated latch value to the second memory location includes latching the second updated latch value in response to at least one control signal.
10. The method of claim 9, wherein the at least one control signal comprises a first complementary control signal indicative of a value of the second data value and a second complementary control signal indicative of a status of the read operation.
11. A method for operating a memory device, comprising:
 - refreshing a normal bit of a byte stored in the memory device; and
 - refreshing a complementary bit of the byte stored in the memory device.
12. The method of claim 11, wherein refreshing the normal bit comprises:
 - receiving first and second control signals at a first latch of the memory device;
 - latching a logic value of the normal bit at a first node in response to the first and second control signals;
 - generating a first update value by performing a logic function on the logic value and a first data value; and
 - transmitting the first update value of the normal bit to an output terminal of the first latch in response to a third control signal.
13. The method of claim 12, further including transmitting the first update value of the normal bit to an output terminal of a second latch in response to a fourth control signal.
14. The method of claim 13, wherein refreshing the complementary bit comprises:
 - receiving the first and fifth control signals at a second latch of the memory device;
 - latching a second update value of the complementary bit at a second node in response to the first and fifth control signals; and
 - transmitting the second update value of the complementary bit to an output terminal of the second latch in response to a sixth control signal.

15. A method for refreshing a memory device, comprising:
 - providing the memory device having a data latch, a complementary data latch, and a write latch;
 - applying first and second control signals to the data latch, wherein the first control signal represents a programming status of a memory location;
 - latching a memory value in the data latch in response to the first and second control signals;
 - performing a logic operation on the memory value and a data value to generate a refresh value;
 - transmitting the refresh value to an output terminal of the write latch;
 - applying the first control signal and a third control signal to the complementary data latch;
 - latching a complementary refresh value in the complementary data latch in response to the first control signal and a third control signal; and
 - transmitting the complementary refresh value to the output terminal of the write latch.
16. The method of claim 15, wherein performing the logic operation on the memory value and the data value includes ORing the memory value and the data value to generate the refresh value.
17. The method of claim 16, further including transmitting the refresh value at the first node of the data latch to an output terminal of the data latch in response to a fourth control signal.
18. The method of claim 17, further including transmitting the logic low level at the first node of the data latch to an output terminal of the write latch in response to a fifth control signal.
19. The method of claim 18, wherein applying the first and third control signals produces a logic low level at a first node of the complementary data latch.

20. The method of claim 19, further including transmitting the logic low level at the first node of the complementary data latch to the output terminal of the data latch in response to the fourth control signal.

21. The method of claim 20, further including transmitting the logic low level at the first node of the complementary data latch to the output terminal of the write latch in response to the fifth control signal.

22. The method of claim 21, wherein the logic low level at the first node of the data latch is produced during the first half of a first clock cycle, the logic low level at the first node of the data latch is transmitted to the output terminal of the write latch during a second half of the first clock cycle, the logic low level at the first node of the complementary data latch is produced during the first half of a second clock cycle, and the logic low level at the first node of the complementary data latch is transmitted to the output terminal of the write latch during a second half of the second clock cycle.

23. A memory device, comprising:

a first latching circuit having an input terminal, a first control terminal coupled for receiving a first control signal, a second control terminal coupled for receiving a second control signal, a third control terminal coupled for receiving a third control signal and an output terminal; and

a second latching circuit having a first control terminal coupled for receiving a first complementary control signal, a second control terminal for receiving a second complementary control signal, a third control terminal coupled for receiving a third complementary control signal, and an output terminal, wherein the output terminal of the second latching circuit is coupled to the output terminal of the first latching circuit to form a common output terminal.

24. The memory device of claim 23, further including a third latching circuit coupled to the common output terminal, the third latching circuit having a first control terminal coupled for receiving a first normal control signal and a second control terminal coupled for receiving a second normal control signal.

25. The memory device of claim 23, further including a first gating circuit coupled to the first latching circuit, the first gating circuit having a first gating control terminal and a data input terminal.
26. The memory device of claim 25, further including a second gating circuit coupled between the common output terminal and the third latching circuit, the second gating circuit having a second gating control terminal.
27. The memory device of claim 23, wherein the second latching circuit comprises a series connected set of transistors having first and second input terminals and an output terminal; and
a latch having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the series connected set of transistors.
28. The memory device of claim 27, wherein the second latching circuit further comprises:
an inverter having an input terminal and an output terminal, the input terminal coupled to the output terminal of the latch; and
a passgate having an input terminal, an output terminal, and a control terminal, wherein the input terminal is coupled to the output terminal of the latch, the output terminal of the passgate serves as the complementary output terminal, and the control terminal is coupled for receiving the third complementary control signal.
29. The memory device of claim 27, wherein the third complementary control signal is a differential control signal.
30. A memory device, comprising:
an input circuit having an input terminal, an output terminal, and an input control terminal;
a latch circuit having an input node and an output terminal, wherein the input node is coupled to the output terminal of the input circuit; and
a complementary latch circuit having a latching node and an output terminal, wherein the output terminal of the complementary latch circuit is commonly connected to the output terminal of the latch circuit.

31. The memory device of claim 30, further including:
a write latch input circuit having an input terminal, and output terminal, and a write latch control terminal; and
a write latch circuit having an input node and an output terminal, wherein input node is coupled to the output terminal of the latch circuit.
32. The memory device of claim 31, wherein the write latch input circuit comprises a passgate having a noninverting control terminal and an inverting control terminal.